IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/699,221	Confirmation No.:	2799
First Named Inventor:	Constantin Bulucea	Filing Date:	31 October 2003
Group Art Unit:	2814	Examiner:	Unknown
Atty. Docket No.:	NS-5127-1D US		
Title:	Gate-Enhanced Junction Varactor With Gradual Capacitance Variation		
Assignee:	National Semiconductor Corporation		

Mountain View, California
9 May 2005

COMMISSIONER FOR PATENTS
PO Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.97(b)

Sir:

Pursuant to 37 CFR 1.56, 1.97, and 1.98, each document listed on the accompanying substitute PTO Form 1449 is called to the attention of the Examiner for the above patent application. A copy of each listed document is enclosed.

Takeuchi et al. is cited on page 59 of the specification of the above application. U.S. Patent Application Publication US 2002/0074589 A1 (Benaissa et al.) was recently cited in parent U.S. patent application 10/054,653 during its prosecution.

Citation of each listed document shall not be construed as:

1. an admission that the document is necessarily prior art with respect to the instant invention;
2. a representation that a search has been made; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 CFR 1.56(b).

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This information disclosure statement is submitted under the provisions of 37 CFR 1.97(b).

EXPRESS MAIL LABEL NO.:
EV 500 310 862 US

Respectfully submitted,

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U.S. Department of Commerce, Patent and Trademark Office	Atty. Docket No.	Application No.
	NS-5127-1D US	10/699,221
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	Confirmation No.
Substitute Form PTO 1449	Bulucea, Constantin	2799
	Filing Date	Group
	31 October 2003	2814

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	2002/0074589	06/2002	Benaissa et al.	257	312	
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AI							
	AJ							
	AK							
	AL							
	AM							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AN	Takeuchi et al, "A New Multiple Transistor Design Methodology for High Speed Low Power SOCs," IEDM Technical Digest, December 2001, pages 22.6.1 - 22.6.7
	AO	
	AP	

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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